In the Claims:

Claims 1-21 (Cancelled).

22. (Previously Presented) A method for operating a watchdog timer associated with a microcontroller that generates refresh commands for the watchdog timer, the refresh commands being separated by a time interval within a predetermined range, the method comprising:

receiving the refresh commands by the watchdog timer; and

generating a microcontroller reset command by the watchdog timer when a time interval separating successively received refresh commands is not within the predetermined range, the generating comprising

starting a refresh countdown on each receipt of a refresh command by the watchdog timer,

starting a reset countdown if the refresh countdown has timed out, and if the refresh countdown has not timed out when a next refresh command is received, then the reset countdown is not restarted, and

generating the microcontroller reset command if the reset countdown has timed out.

23. (Previously Presented) A method according to Claim 22, wherein the reset countdown is restarted only if the refresh countdown has timed out; and a duration of the reset countdown is equal to a maximum time period of the predetermined range, and a duration of the refresh countdown is equal to a minimum time period of the predetermined range.

24. (Previously Presented) A method according to Claim 22, wherein the reset countdown is restarted only if the refresh countdown has timed out when the next refresh command is received; and a duration of the reset countdown is equal to the maximum time period of the predetermined range, and a duration of the refresh countdown is equal to the minimum time period of the predetermined range.

25. (Previously Presented) A method according to Claim 24, wherein if the refresh countdown has timed out, then the reset countdown and the refresh countdown are restarted simultaneously on receipt of the next refresh command.

26. (Previously Presented) A method according to Claim 22, wherein the reset countdown is synchronized with a frequency divided clock signal.

27. (Previously Presented) A method according to Claim 22, wherein the refresh countdown is synchronized with a clock signal.

28. (Previously Presented) A method according to Claim 22, further comprising programming duration of the reset countdown.

29. (Previously Presented) A method according to Claim 28, wherein the watchdog timer comprises a refresh counter for performing the refresh countdown; and wherein the refresh command is received by the refresh counter for

defining the duration of the reset countdown.

30. (Previously Presented) A method according to Claim 29, wherein the watchdog timer comprises a reset counter for performing the reset countdown and is connected to the refresh counter; and wherein the refresh command comprises a word having a plurality of bits, the word being written in the reset counter for defining the duration of the reset countdown.

31. (Previously Presented) A method according to Claim 22, wherein the watchdog timer comprises a reset counter for performing the reset countdown; and wherein the reset counter comprises a plurality of bits including a high-order bit, and the microcontroller reset command is generated by transition of the high-order bit to a low logic value.

32. (Previously Presented) A watchdog timer for a microcontroller that generates refresh commands for the watchdog timer, the refresh commands being separated by a time interval within a predetermined range, the watchdog timer comprising:

a refresh counter comprising a refresh input for receiving the refresh commands from the microcontroller, said refresh counter starting a refresh countdown on each receipt of a refresh command at the refresh input, and generating a refresh command on expiration of the refresh countdown; and

a reset counter comprising a refresh input and a reset output, said reset counter starting a reset countdown on receipt of the refresh command generated by said refresh

counter, and generating a microcontroller reset command at the reset output when the reset countdown times out.

33. (Previously Presented) A watchdog timer according to Claim 32, wherein said refresh counter only generates a refresh command for restarting said reset counter when the refresh countdown has timed out; and a duration of the reset countdown is equal to a maximum time period of the predetermined range, and a duration of the refresh countdown is equal to a minimum time period of the predetermined range.

34. (Previously Presented) A watchdog timer according to Claim 32, wherein said refresh counter only generates a refresh command for restarting said reset counter when the refresh countdown has timed out and a next refresh command is received by said refresh counter; and a duration of the reset countdown is equal to the maximum time period of the predetermined range, and a duration of the refresh countdown is equal to the minimum time period of the predetermined range.

35. (Previously Presented) A watchdog timer according to Claim 32, wherein said reset counter comprises a plurality of bits including a high-order bit connected to the reset output.

36. (Previously Presented) A watchdog timer according to Claim 35, wherein said reset counter comprises a register.

37. (Previously Presented) A watchdog timer according to Claim 36, further comprising an activation input, and a logic circuit having a first input connected to the activation input and a second input connected to the reset output of said reset counter.

38. (Previously Presented) A watchdog timer according to Claim 37, wherein said register comprises a register activation bit connected to the activation input.

39. (Previously Presented) A watchdog timer according to Claim 32, further comprising:

a timer input; and

a frequency divider having an input connected to the timer input, and an output connected to said reset counter for decrementing said reset counter when a signal is applied thereto by said frequency divider.

40. (Previously Presented) A watchdog timer according to Claim 39, wherein duration of the refresh countdown is less than a time period separating two decrements of said reset counter.

41. (Previously Presented) A watchdog timer according to Claim 39, wherein said refresh counter is connected to the timer input for receiving a clock signal, said refresh counter comprising a plurality of bits and being decremented when the clock signal is applied thereto.

42. (Previously Presented) A watchdog timer

according to Claim 32, wherein duration of the reset countdown is programmable.

43. (Previously Presented) An electronic circuit comprising:

a microcontroller generating refresh commands, the refresh commands being separated by a time interval within a predetermined range; and

a watchdog timer connected to said microcontroller for receiving the refresh commands and comprising

a refresh counter comprising a refresh input for receiving the refresh commands from the microcontroller, said refresh counter starting a refresh countdown on each receipt of a refresh command at the refresh input, and generating a refresh command on expiration of the refresh countdown, and

a reset counter comprising a refresh input and a reset output, said reset counter starting a reset countdown on receipt of the refresh command generated by said refresh counter, and generating a microcontroller reset command at the reset output when the reset countdown times out.

44. (Previously Presented) An electronic circuit according to Claim 43, wherein said refresh counter only generates a refresh command for resetting said reset counter when the refresh countdown has timed out; and a duration of the reset countdown is equal to a maximum time period of the

predetermined range, and a duration of the refresh countdown is equal to a minimum time period of the predetermined range.

45. (Previously Presented) An electronic circuit according to Claim 43, wherein said refresh counter only generates a refresh command for resetting said reset counter when the refresh countdown has timed out and a next refresh command is received by said refresh counter; and a duration of the reset countdown is equal to the maximum time period of the predetermined range, and a duration of the refresh countdown is equal to the minimum time period of the predetermined range.

46. (Previously Presented) An electronic circuit according to Claim 43, wherein said reset counter comprises a plurality of bits including a high-order bit connected to the reset output.

47. (Previously Presented) An electronic circuit according to Claim 46, wherein said reset counter comprises a register.

48. (Previously Presented) An electronic circuit according to Claim 47, further comprising an activation input, and a logic circuit having a first input connected to the activation input and a second input connected to the reset output of said reset counter.

49. (Previously Presented) An electronic circuit according to Claim 48, wherein said register comprises a

register activation bit connected to the activation input.

50. (Previously Presented) An electronic circuit according to Claim 43, further comprising:

a timer input; and

a frequency divider having an input connected to the timer input, and an output connected to said reset counter for decrementing said reset counter when a signal is applied thereto by said frequency divider.

51. (Previously Presented) An electronic circuit according to Claim 50, wherein duration of the refresh countdown is less than a time period separating two decrements of said reset counter.

52. (Previously Presented) An electronic circuit according to Claim 50, wherein said refresh counter is connected to the timer input for receiving a clock signal, said refresh counter comprising a plurality of bits and being decremented when the clock signal is applied thereto.

53. (Previously Presented) An electronic circuit according to Claim 43, wherein duration of the reset countdown is programmable.